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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,829	03/30/2004	Kenya Uesugi	57810-098	3066
7590	05/17/2007	McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096	EXAMINER SITTA, GRANT	
ART UNIT	PAPER NUMBER	2609		
MAIL DATE	DELIVERY MODE	05/17/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/811,829	UESUGI ET AL.
Examiner	Art Unit	
Grant D. Sitta	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 30 March 2004.
- 2a) This action is FINAL.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-19 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date <u>3/30/2004</u> .	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the legal term "comprises" is used. It is suggested to change to "includes". See MPEP 608.01(b).

3. The abstract of the disclosure is objected to because "The display is provide with..." should be "The display is provided with...". Correction is required. See MPEP § 608.01(b).

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The term "type" in claims 1 is a relative term which renders the claim indefinite.

The term "type" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

7. Claim 2 recites the limitation " set such that the moment said first transistor" in claim 2 line 3. There is insufficient antecedent basis for this limitation in the claim. "the moment" must refer to a "moment" in a preceding related claim. However, claim 2 is the first instance of a "moment."

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1,5,7-8, 10, 12-13, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Okumura et al (U.S. 4,587,446) hereinafter Okumura.

In regards to claim 1, a first transistor (Fig. 3 T25) of first conductivity type connected to a first potential side (Fig. 3 VCC) and turned on in response to a clock signal (Fig. 3 A);

a second transistor of first conductivity type (Fig. 3, T26) connected to a second potential side (Fig. 3 GROUND);

a third transistor of first conductivity type (Fig. 3 T24) connected between a gate of said first transistor and said second potential; and

a high resistance (Fig. 2 T21, T23 or R1) connected between the gate of said first transistor (Fig. 3 T25) and a clock signal (Fig. 3 A and A') line supplying said clock signal (col. 6, lines 15-55).

10. In regards to claim 5, first circuit part (Fig. 3) further comprises a diode-connected fourth transistor (Fig. 3) connected between the gate of said first transistor

(Fig. 3 T25) and said clock signal line (Fig. 3 A) and having an on-resistance lower than that of said third transistor. (col. 4, lines 35-50)

11. In regards to claim 7, where the fourth transistor has two gates electrodes electrically connected to each other(Fig. 3 T 22 and T 25).
12. In regards to claim 8, first circuit part (Fig. 3) further comprises a fourth transistor connected (T23) between the gate ( Fig. 3 gate T25) of said first transistor and said clock signal line (Fig. 3 A) and turned on in response to a signal by which a period of on state which does not overlap with a period of on state of said third transistor is provided (Fig. 3 T24).
13. In regards to claim 10, a diode-connected fifth transistor connected between said fourth transistor and said clock signal line (Fig. 3 T22). Examiner notes a resistor is often substituted for a diode-connected transistor and R1 may also satisfy these requirements of clock A'.
14. In regards to claim 12, a capacitor is connected between the gate and the source of said first transistor (Fig. 3 C3)
15. In regards to claim 13, a third transistor (Fig. 3 T24) has a function of turning said first transistor off when said second transistor (Fig. 3 T26) is in an on state. (col. 4, lines 50-70).
16. In regards to claim 15, third transistor has two gate electrodes connected to each other. (Fig. 3 (T24 and T27))
17. In regards to claim 17, shift register comprises (Fig. 3) a shift register circuit for driving a drain line to which a picture signal is supplied (col. 3, lines 50-55, "data input")

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 2,3,4,6,9,11,14,16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Miyatake et al (US 2002/0075222) hereinafter Miyatake.

21. In regards to claim 2, Okumura discloses the limitations of claim 1. Okumura differs from the claimed invention in that Okumura does not disclose such that the moment said first transistor of a predetermined stage of shift register circuit is switched from off state to on state may not overlap with the moment said first transistor of the shift register circuit two stages prior to the predetermined stage is switched from on state to off state.

However, Miyatake teaches a system and method for driving a display such that the moment said first transistor of a predetermined stage of shift register circuit is switched from off state to on state may not overlap with the moment said first transistor of the shift register circuit two stages prior to the predetermined stage is switched from on state to off state Fig. 4 A([0067]) (Out (N-1), Out (N+1)).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Okumura to include the use of staggered analog switching as taught by Miyatake in order to prevent display irregularities as stated in ([0021] of Miyatake).

22. In regards to claim 3, the high resistance has a value set such that the first transistor of the predetermined stage of shift register circuit is turned on, after said first transistor of the shift register circuit two stages prior to the predetermined stage was turned off. Fig. 4 A([0067]) (Out (N-1), Out (N+1)).

23. In regards to claim 4, corresponding to said first potential is output from said first circuit part through said first transistor (Fig. 3 T25, Okumura), and an output signal of said first circuit part (Fig. 5, Out (N-1), Miyatake) of the predetermined stage of shift register circuit is switched from said second potential (Ground, Okumura) to said first potential (Vcc, Okumura), after an output signal (Fig. 4, Out (N-1), Out, Out (N+1) of said first circuit part of the shift register circuit two stages prior to the predetermined stage was switched from said first potential (Vcc Okumura) to said second potential (Ground, Okumura), (Fig. 4 Miyatake).

24. In regards to claim 6, where the fourth transistor is a p-type field effect transistor. (Col. 3 lines 10-25). Examiner notes it would be an obvious matter of design choice to make use a p-type field effect transistor. Since Okumura already mentions using field effect transistors it would have been a mere change from an n-type.

25. In regards to claim 9, see claim 6.

26. In regards to claim 11, see claim 6.

27. In regards to claim 14, see claim 6.

28. In regards to claim 16, first circuit part is arranged in an output side of a shift register (Fig 3. Area between T25 and T26) and

A second circuit part comprising said first transistor, said second transistor (Fig. 3, T26), said second transistor (Fig. 3, T26) and said third transistor (Fig. 3 T24) but not comprising said high resistance (Fig. 2 T21, T23 or R1) is arranged on an input side of said signal register circuit (Fig. 3 I). Examiner notes it would have been obvious matter of design choice to modify Okumura reference by having the components in certain groups, since applicant has not disclosed that having the transistors at this specific grouping solves any stated problem or is for any particular purpose and it appears that invention disclosed by Okumura would perform equally well within the disclosed arrangement.

29. In regards to claim 18, a drain line driven by said shift register circuit (Fig 1, 1 and 64, Miyatake) has a function of supplying said picture signal to a display pixel comprising a liquid crystal (Fig. 1 61).

30. In regards to claim 19, said drain line driven by said shift register circuit has a function of supplying said picture signal to display pixel comprising an organic EL element. (Fig. 1 Miyatake). Examiner notes it would have been obvious to substitute an organic EL means for LCD of reference Miyatake since it has generally been recognized that the substitution of a LCD for an organic EL involves only routine skill in the art. *IN re Vanner*, 120 USPQ 193 (CCPA 1958).

#### Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

May 7, 2007

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